WHAT IS CLAIMED IS:

Sub A2

1. A processor including a memory, a plurality of execution units coupled to the memory and an array prefetch apparatus for transferring array data from the memory to the plurality of execution units in the processor, the array prefetch apparatus comprising:

an array prefetch queue coupled to the memory for receiving array data;

a first array prefetch queue pointer coupled to the array prefetch queue for designating in the array prefetch queue a location for loading the array data;

a second array prefetch queue pointer coupled to the array prefetch queue for designating in the array prefetch queue a location for accessing the array data;

an array prefetch controller coupled to the array prefetch queue and the first and second array prefetch queue pointers, the array prefetch controller for executing a load operation as an array load operation and an array move operation, the array load operation for accessing the array data from the memory and transferring the array data to the array prefetch queue at the location designated by the first pointer, the array move operation for moving the array data from the array prefetch queue at the location designated by the second pointer for accessing by the execution units of the processor.

2. A processor according to Claim 1 wherein the array load operation and the array move operation are executed independently and asynchronously.

3. A processor according to Claim 1 further comprising:

an array prefetch flag register coupled to the array prefetch controller, the array prefetch flag selectively directing the array prefetch controller to execute the load operation as the array load operation and the array move operation for a first array prefetch flag register setting and to execute the load operation as a load operation for a second array prefetch flag register setting.

4. A processor according to Claim 1 wherein the array load operation inherits attributes of the load operation that concern issuing of a memory request and advancing of a memory address and wherein the array move operation inherits attributes of the load operation that concern loading of a destination register by a read data.

~~5. A processor according to Claim 1 further comprising a loop control logic supporting software pipelining of loops, the loop control logic for executing a plurality of stages (S) in a compiled, pipelined loop schedule of T cycles having an iteration interval I, in which the loop control logic dynamically controls the number of stages in an iteration as a function of the latencies of memory read operations.~~

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~~6. A processor according to Claim 1, further comprising:~~

~~a loop control logic supporting software pipelining of loops in a horizontal processor, the loop control logic including:~~

~~a loop mode flag indicative of a current loop mode status, the loop mode flag being set when a loop is executed;~~

~~a loop counter indicative of a first remaining number of logical iterations in the loop being executed;~~

~~a prologue counter indicative of a second remaining number of logical iterations in a prologue portion of the loop being executed; and~~

~~first enabling/disabling logic coupled to the loop mode flag and to the prologue counter, the first enabling/disabling logic disabling execution of operations in a first class of operations having side effects.~~

5 ~~7.~~ A processor according to Claim 1, wherein the array prefetch queue further comprises:

an array prefetch queue data memory; and

an array prefetch queue for valid bits.

6 ~~8.~~ A processor according to Claim 1, further comprising:

a plurality of array access channels, wherein the array prefetch queue further comprises:

an array prefetch queue data memory including a plurality of channels, the channels of the array prefetch data memory corresponding one-to-one to the array access channels; and

an array prefetch queue for valid bits including a plurality of channels, the channels of the array prefetch queue for valid bits corresponding one-to-one to the array access channels.

15 ~~9~~. A processor including an array prefetch apparatus for transferring array data from a memory to a register, the array prefetch apparatus comprising:

an array prefetch queue coupled to the memory for receiving the array data;

an array prefetch queue tail pointer coupled to the array prefetch queue for designating in the array prefetch queue a location for loading the array data;

an array prefetch queue head pointer coupled to the array prefetch queue for designating in the array prefetch queue a location for accessing the array data and moving the array data to a register;

an array prefetch flag;

an array prefetch controller coupled to the array prefetch queue, the array prefetch flag and the first and second array prefetch queue pointers, the array prefetch controller for executing a load operation as a load operation for a first setting of the array prefetch flag and alternatively, for a second setting of the array prefetch flag, executing a load operation as a combination of an array load operation and an array move operation, the array load operation for accessing the array data from the memory and transferring the array data to the array prefetch queue at the location designated by the array prefetch queue tail pointer, the array move operation for moving the array data from the array prefetch queue at the location designated by the array prefetch head pointer to a register designated by the array move operation.

16 ~~10.~~ A processor according to Claim ~~9,~~ 15 wherein the array load operation inherits attributes of the load operation that concern issuing of a memory request and advancing of a memory address and wherein the array move operation inherits attributes of the load operation that concern loading of a destination register by a read data.

17 ~~11.~~ A processor according to Claim ~~9~~ 15 wherein the array load operation and the array move operation are executed independently and asynchronously.

~~12. A processor according to Claim 9 further comprising a loop control logic supporting software pipelining of loops, the loop control logic for executing a plurality of stages (S) in a compiled, pipelined loop schedule of T cycles having an iteration interval I, in which the loop control logic dynamically controls the number of stages in an iteration as a function of the latencies of memory read operations.~~

~~13. A processor according to Claim 9, further comprising:~~

~~a loop control logic supporting software pipelining of loops in a horizontal processor, the loop control logic including:~~

~~a loop mode flag indicative of a current loop mode status, the loop mode flag being set when a loop is executed;~~

~~a loop counter indicative of a first remaining number of logical iterations in the loop being executed;~~

~~a prologue counter indicative of a second remaining number of physical iterations in a prologue portion of the loop being executed; and~~

~~first enabling/disabling logic coupled to the loop mode flag and to the prologue counter, the first enabling/disabling logic disabling execution of operations in a first class of operations having side effects.~~

Sub B4

14. A method of transferring array data from a memory to a register comprising the steps of:

designating in an array prefetch queue a location for loading array data;

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~~designating in the array prefetch queue a location for accessing the array data and moving the array data to a register;~~

~~executing a load operation as a combination of an array load operation and an array move operation;~~

~~for the array load operation, accessing the array data from the memory and transferring the array data to the array prefetch queue at the location for loading array data;~~

~~for the array move operation, moving the array data from the array prefetch queue at the location designated by the second pointer to a register designated by the array move operation.~~

8 ~~15~~. A method according to Claim ~~14~~ 7 further comprising:

executing a load operation as a combination of an array load operation and an array move operation for a first setting of an array prefetch flag; and

alternatively executing a load operation as a load operation for a second setting of an array prefetch flag.

9 ~~16~~. A method according to Claim ~~14~~ 7 wherein the array load operation and the array move operation are executed independently and asynchronously.

10 ~~17~~. A method according to Claim ~~14~~ 7, wherein the array load operation inherits attributes of the load operation that concern issuing of a memory request and advancing of a memory address and wherein the array move operation inherits attributes of the load operation that concern loading of a destination register by a read data.

11 ~~18~~. A method of providing a processor including an array prefetch apparatus for transferring array data from a memory to a register, the array prefetch apparatus comprising the steps of:

providing an array prefetch queue coupled to the memory for receiving the array data;

providing an array prefetch queue tail pointer coupled to the array prefetch queue for designating in the array prefetch queue a location for loading the array data;

providing an array prefetch queue head pointer coupled to the array prefetch queue for designating in the array prefetch queue a location for accessing the array data and moving the array data to a register;

providing an array prefetch flag;

providing an array prefetch controller coupled to the array prefetch queue, the array prefetch flag and the first and second array prefetch queue pointers, the array prefetch controller for executing a load operation as a load operation for a first setting of the array prefetch flag and alternatively, for a second setting of the array prefetch flag, executing a load operation as a combination of an array load operation and an array move operation, the array load operation for accessing the array data from the memory and transferring the array data to the array prefetch queue at the location designated by the array prefetch queue tail pointer, the array move operation for moving the array data from the array prefetch queue at the location designated by the array prefetch head pointer to a register designated by the array move operation.

12 ~~19~~. A method according to Claim 11 ~~18~~, wherein the array load operation inherits attributes of the load operation that concern issuing of a memory request and advancing of a memory address and wherein the array move operation inherits attributes of the load operation that concern loading of a destination register by a read data.

13 ~~20~~. A method according to Claim 11 ~~18~~, wherein the array load operation and the array move operation are executed independently and asynchronously.

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